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Complete 12-bit, 25MSPS Monolithic A/D Converter
AD9225

FEATURES
Monolithic 12-bit, 25MSPS A/D Converter
Low Power Dissipation: 300mW
Single +5V Supply
No Missing Codes Guaranteed
Differential Nonlinearity Error: ±0.5 LSB
Complete: On-Chip Sample-and-Hold Amplifier and
**   Voltage Reference**
Signal-to-Noise and Distortion Ratio: 70 dB
Spurious-Free Dynamic Range: 85 dB
Out of Range Indicator
Straight Binary Output Data
28 Pin SSOP

FUNCTIONAL BLOCK DIAGRAM

PRODUCT DESCRIPTION
The AD9225 is a monolithic, single supply 12-bit, 25MSPS Analog to Digital Converter with an on-chip, high performance sample-and-hold amplifier and voltage reference. The AD9225 uses a multi-stage differential pipelined architecture with output error correction logic to provide 12-bit accuracy at 25MSPS data rates and guarantees no missing codes over the full operating temperature range.

The AD9225 combines a low cost high-speed CMOS process and a novel architecture to achieve the resolution and speed of existing hybrid implementations at a fraction of the power consumption and cost.
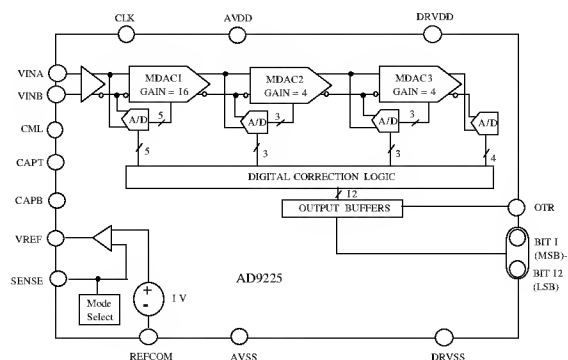
The input of the AD9225 allows for easy interfacing to both imaging and communications systems. With a truly differential input structure, the user can select a variety of input ranges and offsets. The dynamic performance is excellent.

The sample-and-hold (SHA) amplifier is well suited for both multiplexed systems that switch fullscale voltage levels in successive channels and sampling single-channel inputs at frequencies up to and well beyond the Nyquist rate.

The AD9225's wideband input combined with the power and cost savings over previously available monolithics and hybrids will enable new design applications in communications, imaging and medical applications.

 The AD9225 has an on board, programmable reference. An external reference can also be chosen

to suit the DC accuracy and temperature drift requirements of the application.

 A single clock input is used to control all internal conversion cycles. The digital output data is presented in straight binary output format. An out-of-range signal indicates an overflow condition which can be used with the most significant bit to determine low or high overflow.

PRODUCT HIGHLIGHTS
The AD9225 is fabricated on a very cost effective CMOS process. High-speed, precision analog circuits are now combined with high density logic circuits.

The AD9225 offers a complete single-chip sampling 12-bit, 25MSPS analog-to-digital conversion function in a 28 pin SSOP package.

Low Power - The AD9225 at 300mW consumes a fraction of the power of presently available hybrids and existing monolithic solutions.

On-Board Sample-and-Hold (SHA) - The versatile SHA input can be configured for either single ended or differential inputs.

OUT OF RANGE (OTR) - The OTR output bit indicates when the input signal is beyond the AD9225's input range.

Single Supply - The AD9225 uses a single +5V power supply simplifying system power supply design. The output drivers can be operated from a separate 3V-5V supply if desired.

AD9225 - DC SPECIFICATIONS

(AV_{DD}=+5V, DRV_{DD}=+5V, f_{SAMPLE} =25MSPS, VREF=2.0V, VINB=2.5Vdc unless otherwise indicated)

PARAMETER	AD9225	Units
RESOLUTION	12	Bits min
MAX CONVERSION RATE	25	MHz min
INPUT REFERRED NOISE		
VREF=1V	.35	LSB RMS typ
VREF=2.0V	.17	LSB RMS typ
ACCURACY		
Integral Nonlinearity (INL)	±1	LSB typ
Differential Nonlinearity (DNL)	±0.5	LSB typ
No Missing Codes	12	Bits Guaranteed
Zero Error (@25°C)	TBD	% FSR typ
Gain Error (@25°C)[1]	TBD	% FSR typ
Gain Error (@25°C)[2]	TBD	% FSR typ
TEMPERATURE DRIFT		
Zero Error	TBD	PPM/°C
Gain Error[1]	TBD	PPM/°C
Gain Error[2]	TBD	PPM/°C
POWER SUPPLY REJECTION		
AV_{DD}, DRV_{DD}(+5V±0.25V)	TBD	% FSR typ
ANALOG INPUT		
Input Span	2	Vp-p min
	4	Vp-p max
Input (Vina or Vinb) Range	0	V min
	AVDD	V max
Input Capacitance	10	pF typ
INTERNAL VOLTAGE REFERENCE		
Output Voltage (1V mode)	1.0	Volts typ
Output Voltage Tolerance (1V mode)	TBD	mV max
Output Voltage (2.0V mode)	2.0	Volts typ
Output Voltage Tolerance (2.0V mode)	TBD	mV max
Output Current (available for external loads) (External load should not change during conversion)	1.0	mA min
REFERENCE INPUT RESISTANCE	5	kΩ typ
POWER SUPPLIES		
Supply Voltages		
AV_{DD}	5	V (±5% AV_{DD} Operating)
DRV_{DD}	5	V (±5% DRV_{DD} Operating)
Supply Current		
IAV_{DD}	TBD	mA typ
$IDRV_{DD}$	TBD	mA typ
POWER CONSUMPTION	300	mW typ

NOTES
1 Includes Internal voltage reference drift
2 Excludes internal voltage reference drift
Specification subject to change without notice.

AD9225 - AC SPECIFICATIONS

(AV_{DD}=+5V, DRV_{DD}=+5 V, f_{SAMPLE} = 25MSPS, VREF = 2.0V, Differential Input unless otherwise indicated)

	AD9225		Units	
SIGNAL-TO-NOISE AND DISTORTION RATIO (S/N+D)				
f_{INPUT}=2.5MHz	70		dB typ	
f_{INPUT}=12.5MHz		68		dB typ
SIGNAL-TO-NOISE RATIO (SNR)				
f_{INPUT}=2.5MHz	71		dB typ	
f_{INPUT}=12.5MHz		TBD		dB typ
TOTAL HARMONIC DISTORTION (THD)				
f_{INPUT}=2.5MHz	-80		dB typ	
f_{INPUT}=12.5MHz		-75		dB typ
SPURIOUS FREE DYNAMIC RANGE				
f_{INPUT}=2.5MHz	85		dB typ	
f_{INPUT}=12.5MHz		-80		dB typ
Full Power Bandwidth	160		MHz typ	
Small Signal Bandwidth	160		MHz typ	
Aperture Delay	1		nS typ	
Aperture Jitter	4		pS RMS typ	
Acquisition to Full Scale Step	TBD		nS typ	
Overvoltage Recovery Time	TBD		nS typ	

AD9225 - DIGITAL SPECIFICATIONS
(AVDD=+5V, DRVDD=+5V unless otherwise indicated)

PARAMETERS	Symbol		Units
LOGIC INPUTS			
High Level Input Voltage	V_{IH}	+3.5	V min
Low Level Input Voltage	V_{IL}	+1.0	V max
High Level Input Current ($V_{IN}=DV_{DD}$)	I_{IH}	+/-10	μA max
Low Level Input Current ($V_{IN}=0V$)	I_{IL}	+/-10	μA max
Input Capacitance	C_{IN}	5	pF typ
LOGIC OUTPUTS			
High Level Output Voltage ($I_{OH}=50\mu$A)	V_{OH}	+4.5	V min
High Level Output Voltage ($I_{OH}=0.5$mA)	V_{OH}	+2.4	V min
Low Level Output Voltage ($I_{OL}=1.6$mA)	V_{OL}	+0.4	V max
Low Level Output Voltage ($I_{OL}=50\mu$A)	V_{OL}	+0.1	V max
Output Capacitance	C_{OUT}	5	pF typ

Specifications subject to change without notice.

SWITCHING SPECIFICATIONS
(T_{min} to T_{max} with AV_{DD}= +5V, DRV_{DD}=+5V, C_L=20pF)

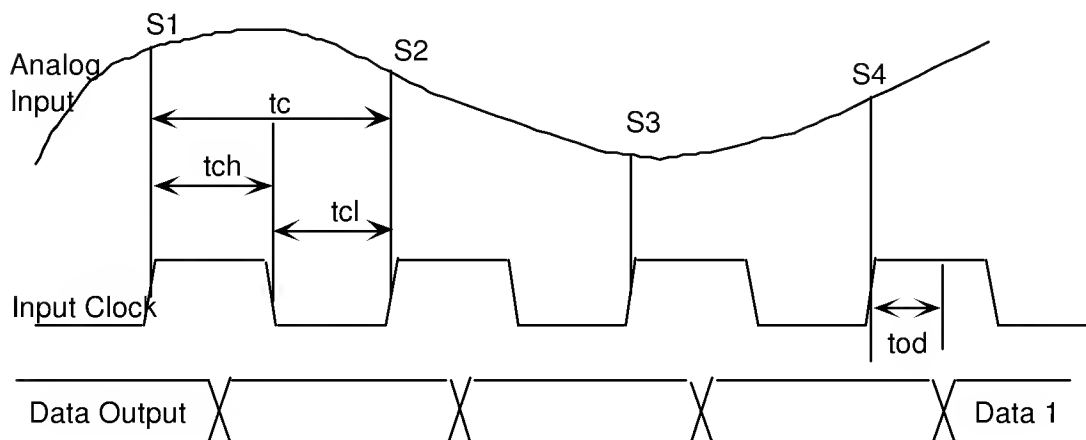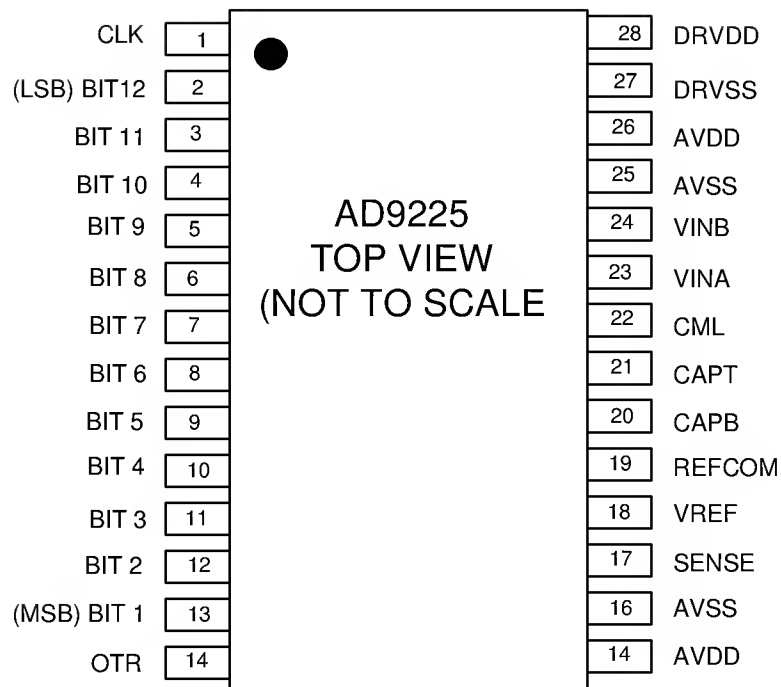| PARAMETERS	Symbol	AD9225	Units
Clock Period[1]	t_C	40	nS min
CLOCK Pulse Width High	t_{CH}	20	nS min
CLOCK Pulse Width Low	t_{CL}	20	nS min
Output Delay	t_{OD}	TBD	nS min(13nS typ)
		TBD	nS max
Pipeline Delay (Latency)		3	Cycles

Figure 1. AD9225 Timing Diagram

NOTE
1 The clock period may be extended to 1 ms without degradation in specified performance @25 C
Specifications subject to change without notice.

CLK ☐ 1
(LSB) BIT12 ☐ 2
BIT 11 ☐ 3
BIT 10 ☐ 4
BIT 9 ☐ 5
BIT 8 ☐ 6
BIT 7 ☐ 7
BIT 6 ☐ 8
BIT 5 ☐ 9
BIT 4 ☐ 10
BIT 3 ☐ 11
BIT 2 ☐ 12
(MSB) BIT 1 ☐ 13
OTR ☐ 14

AD9225 TOP VIEW (NOT TO SCALE

28 ☐ DRVDD
27 ☐ DRVSS
26 ☐ AVDD
25 ☐ AVSS
24 ☐ VINB
23 ☐ VINA
22 ☐ CML
21 ☐ CAPT
20 ☐ CAPB
19 ☐ REFCOM
18 ☐ VREF
17 ☐ SENSE
16 ☐ AVSS
14 ☐ AVDD

PIN DESCRIPTION

Name	Description	SSOP
CLK	Clock Input	1
Bit 12	Least Significant Data Bit (LSB)	2
Bit 11-2	Data Output Bit	3-12
Bit 1	Most Significant Data Bit (MSB)	13
OTR	Out of Range	14
AVDD	+5V Analog Supply	15,26
AVSS	Analog Ground	16,25
SENSE	Reference Select	17
VREF	Input Span Select Reference I/O	18
REFCOM	Reference Common	19
CAPB	Noise Reduction Pin	20
CAPT	Noise Reduction Pin	21
CML	Common Mode Level (Mid Supply)	22
VINA	Analog Input Pin (+)	23
VINB	Analog Input Pin (-)	24
DRVSS	Digital Output Driver Ground	27
DRVDD	+3 to +5 V Digital Output Driver Supply	28

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AVDD	AVSS	-.03	+6.5	V
DRVDD	DRVSS	-0.3	+6.5	V
AVSS	DRVSS	-0.3	+0.3	V
AVDD	DRVDD	-6.5	+6.5	V
REFCOM	AVSS	-0.3	+0.3	V
CLK	AVSS	-0.3	AVDD + 0.3	V
Digital Outputs	DRVSS	-0.3	DRVDD + 0.3	V
VINA,VINB	AVSS	-0.3	AVDD + 0.3	V
VREF	AVSS	-0.3	AVDD + 0.3	V
SENSE	AVSS	-0.3	AVDD + 0.3	V
CAPB, CAPT	AVSS	-0.3	AVDD + 0.3	V
Junction Temperature			+150	°C
Storage Temperature		-65	+150	°C
Lead Temperature (10 Sec)			+300	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

PRELIMINARY